

APPLICANT(S): Gil VINITZKY  
SERIAL NO.: 09/586,775  
FILED: June 5, 2000  
Page 7

**Remarks:**

The present response is intended to be fully responsive to all points raised by the Examiner and is believed to place the application in condition for allowance. Allowance of the application is respectfully requested.

**Abstract**

The abstract of the disclosure has been objected to because the abstract exceeds 150 words in length. The abstract has been amended and currently is 140 words in length, thus curing the objection. Applicants respectfully submit that the amendments to the abstract do not add new matter.

**Status of Claims**

Claims 1 – 6 are pending in the application. Claims 1 – 2 are rejected. Claim 1 has been amended. New claims 3 – 6 have been added. Applicants respectfully submit that these amendments and new claims do not add new matter.

**Claim Rejections – 35 USC 112**

Claims 1 – 2 are rejected under 35 USC 112, second paragraph. The Office Action states that the recitation of “the parity” in line 9 of claim 1 lacks antecedent basis. The Office Action states that claim 2 has been rejected under 35 USC 112, second paragraph for being dependent upon the rejected claim 1.

Claim 1 has been amended to recite “a parity” in line 9, thus overcoming the rejection. Consequently, the rejection of claim 2 has been overcome.

**Claim Rejections – 35 USC 102**

Claims 1 – 2 are rejected under 35 USC 102(b) as being anticipated by Hancke et al. (U.S. Patent No. 3,673,399). Applicant respectfully traverses the rejection, in view of the remarks that follow.

As is well established, in order to successfully assert a *prima facie* case of anticipation, the Examiner must provide a single prior art document that includes every element and limitation of the claim or claims being rejected.

According to Hancke et al., the operands for Pass 1 of the Fast Fourier Transform (FFT) are read from input buffer memory 60 (Fig. 6), which is part of input buffer 23 (Fig. 1). After Pass 1 of the FFT is performed by arithmetic unit (AU) 21, the calculated operands

APPLICANT(S): Gil VINITZKY  
SERIAL NO.: 09/586,775  
FILED: June 5, 2000  
Page 8

(which are the operands of Pass 2) are stored in output buffers 24 and 25. This is evident from the following passage: "During Pass 1, of the processing mode, data is read from input buffer memory 60. ... After each read operation from input buffer memory 60 the operands  $B_r$  and  $C_r$  are clocked into the AU 21 where the first set of operands  $A_r$  and  $A_{r+n/2}$  are computed. The computed operands  $A_r$  and  $A_{r+n/2}$  are then gated through output switch gates 28 and placed in output buffers 24 and 25, as shown in Table II." (col. 10, lines 30-49)

In particular, the computer operands  $A_r$  and  $A_{r+n/2}$  are not stored in the memory space from which the operands  $B_r$  and  $C_r$  were fetched, i.e. are not stored in input buffer 60. Therefore, Hancke et al. does not teach, either expressly or inherently, "*storing ... the results of an FFT operation upon said first data point at the memory address in said first memory space X from which said first data point was fetched and the result of an FFT operation upon said second data point at the memory address in said second memory space Y from which said second data point was fetched*", as recited by claim 1. Similarly, Hancke et al. does not teach, either expressly or inherently, "*storing ... the results of an FFT operation upon said first data point at the memory address in said second memory space Y from which said second data point was fetched and the result of an FFT operation upon said second data point at the memory address in said first memory space X from which said first data point was fetched*", as recited by claim 1.

Hancke et al. fails to teach, either expressly or inherently, the above-quoted limitations of claim 1. Therefore Hancke et al. cannot anticipate claim 1, and the Office Action has failed to establish a *prima facie* case of anticipation.

#### **Remarks to cited reference**

37 CFR 1.111(c) requires an Applicant to clearly point out the patentable novelty which Applicant thinks the newly added claims present in view of the state of the art disclosed by the references cited. According to MPEP 714.02 and 714.04, Applicant is to clearly point out the patentable novelty of a newly added claim by specifically pointing out how the language of the claim patentably distinguishes the claim from the references cited, in order to provide a complete prosecution record as to why the claim should be allowed over the prior art of record. Applicant has presented such arguments below.

Hancke et al. neither teaches nor suggests, *inter alia*, the following limitation of claim 3: "*storing a first output data point of said first stage at said first address in said first memory space*", where 'said first address' is described by "*a first data point of a pair of input data points of a first stage of a Fast Fourier Transform calculation is stored in a first memory space at a first address*". Therefore Hancke et al. cannot anticipate claim 3. Since claim 4 depends from and includes all the limitations of claim 3, Hancke et al. cannot anticipate claim 4.

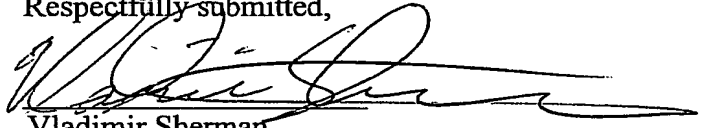
Hancke et al. neither teaches nor suggests, *inter alia*, the limitation of claim 5 "*determining ... whether to store an output data point of a first stage of a Fast Fourier Transform calculation in a first memory space at a first address or in a second memory space at a second address, where a first data point of a pair of input data points of said first stage is stored in said first memory space at said first address and a second data point of said pair is stored in said second memory space at said second address*". Therefore Hancke et al. cannot anticipate claim 5.

Hancke et al. neither teaches nor suggest, *inter alia*, the limitation of claim 6 "means for determining ... whether to store an output data point of said first stage in said first memory space at said first address or in said second memory space at said second address", where 'said first address' and 'said first memory space' are described by "*a first memory space to store a first data point of a pair of input data points of a first stage of a Fast Fourier Transform calculation at a first address*" and 'said second address' and 'said second memory space' are described by "*a second memory space to store a second data point of said pair at said second address*". Therefore Hancke et al. cannot anticipate claim 6.

APPLICANT(S): Gil VINITZKY  
SERIAL NO.: 09/586,775  
FILED: June 5, 2000  
Page 10

Should the Examiner have any question or comment as to the form, content or entry of this Amendment, the Examiner is requested to contact the undersigned at the telephone number below. Similarly, if there are any further issues yet to be resolved to advance the prosecution of this application to issue, the Examiner is requested to telephone the undersigned counsel.

Respectfully submitted,

A handwritten signature in black ink, appearing to read 'Vladimir Sherman', written over a horizontal line.

Vladimir Sherman  
Attorney for Applicant  
Registration No. 43,116

Dated: June 9, 2003

**Eitan, Pearl, Latzer & Cohen Zedek, LLP.**  
10 Rockefeller Plaza, Suite 1001  
New York, New York 10020  
Tel: (212) 632-3480  
Fax: (212) 632-3489